A High Power Density Single-Phase Inverter Using Stacked Switched Capacitor Energy Buffer

Introduction:

Single-phase, high power factor inverters inherently require energy storage to buffer the difference between their instantaneous input and output power. For a variety of applications including single-phase photovoltaic (PV) inverters and uninterruptible power supplies (UPS), the input power drawn by the inverter is required to be constant, with small ripple, while the output power pulsates at twice the line frequency, warranting the need for an intermediate energy storage element. Typically, electrolytic capacitors are utilized as the energy storage element on the dc side to buffer the twice line frequency energy. In conventional inverter architectures, these capacitors are directly connected across the input dc bus. A limitation on the dc bus voltage ripple imposes constraints on the energy utilization of the buffering capacitor. In order to have acceptable voltage ripple on the dc bus, a large capacitor is needed, resulting in poor energy utilization and a substantial fraction of the total volume being utilized for energy buffering.

Existing system:

Further enhancements in inverter power density require a compact and efficient dc-ac power conversion stage. Traditional PWM based dc-ac converters operate in continuous conduction mode (CCM) in high power applications, and in discontinuous/boundary conduction mode (DCM/BCM) for mid and low power designs. Operating in DCM/BCM has several advantages, including smaller
filtering inductors and soft-switching capability. However, conventional DCM/BCM control techniques suffer from reduced efficiencies at low power levels, resulting in low weighted efficiencies.

**Drawbacks:**
- Low weighted efficiencies.
- Resulting in poor energy utilization and a substantial fraction of the total volume being utilized for energy buffering.

**Proposed system:**
A single-phase, high efficiency, high power density 2 kW inverter. For twice-line-frequency energy buffering, this inverter utilizes an advanced variant of the stacked switched capacitor energy buffer architecture. For the dc-ac conversion stage, a high frequency, SiC-MOSFET based solution using variable frequency constant peak current control is utilized. It comprises a stacked switched capacitor (SSC) energy buffer across the dc input bus, and a dc-ac converter utilizing a digital implementation of variable frequency constant peak current control. The following subsections discuss the operational principles of the SSC energy buffer and the dc-ac converter.
Topology of a $n \times m$ enhanced bipolar SSC energy buffer.

DC-AC converter architecture.

**Advantages:**
- Smaller filtering inductors.
- Soft-switching capability.
- High efficiency.
- High power density.

**Applications:**
- Single-phase photovoltaic (PV) inverters.
- Uninterruptible power supplies (UPS).
Block diagram:

Input DC Supply → Energy Buffer → DC-AC Converter → EMI Filter → Load

12V DC → Driver Circuit

5V DC → Buffer Circuit → Micro Controller Circuit