Dual-Calibration Technique for Improving Static Linearity of Thermometer DACs for I/O

Abstract:

In this paper, we propose a dual-calibration technique to improve the matching accuracy of digital-to-analog converter (DAC) elements and improve nonlinearity induced static errors in a current-steering thermometer DAC. The novelty of the proposed dual-calibration scheme lies in obtaining best samples from the error distribution using redundancy for improved matching followed by adaptively reordering these samples to reduce error accumulation. This technique exploits the 2-D nature of the DAC to achieve lower calibration time. We consider the statistical basis for each of these methods and demonstrate statistical modeling of the proposed technique. We demonstrate a 38% reduction in differential nonlinearity (DNL) and 55% reduction in integral nonlinearity (INL) through simulations. We fabricated an 8-bit current steering thermometer DAC in Taiwan Semiconductor Manufacturing Company 65-nm CMOS process. With only 2 redundant cells per row, we show an improvement of 36% in DNL and 50% in INL from the measurement of 16 chips over the baseline DAC. The proposed architecture of this paper the area and power consumption are analysis using tanner tools.

Enhancement of the project:

Change the technology based on the error reduction.

Existing System:

As transistor sizes decrease with the scaling of CMOS processes, the area of a DAC’s unit cell and the overall DAC area also decrease. However, for a given process, matching accuracy among the unit cells is inversely proportional to area. This implies that unit cells need to be made larger to overcome the detrimental effect of increased nonlinearity and to maintain yield. Various preprocessing techniques such as special layout implementations, and biasing and routing schemes have been used to compensate for this loss in accuracy without growing the unit cells. These approaches are good for removing systematic geometric errors. However, they are not able to eliminate random mismatch errors that are becoming dominant in lower feature sizes. Hence, calibration becomes essential.
Calibration schemes for thermometer DACs fall mainly into two categories—trimming and switching. Trimming-based calibration methods focus on decreasing the mismatch error by calibrating each current source to a reference current using a calibration DAC. The issue with most of these schemes is the large amount of area added to the unit cells in the form of additional circuitry that does not scale well with process. Switching-based calibration methods focus on minimizing error accumulation by achieving mismatch error cancellation with successive addressing. Methods like dynamic element matching, which also increases the noise floor, and dynamic mismatch mapping, target dynamic linearity and do not reduce the overall power of the mismatch error that is important for improving the static linearity. Many other switching schemes use complex optimization algorithms requiring higher calibration time and power. In addition, no significant reduction in the mismatch error itself is achieved by the existing switching-based techniques.

Disadvantages:

- Mismatch between the DAC’s unit elements

Proposed System:
The Master of IEEE Projects

Fig. 1. Complete 8-bit dual-calibrated thermometer DAC architecture with all the calibration blocks and modified unit cell (shaded blocks used only during calibration).

The complete dual-calibrated DAC architecture is shown in Fig. 1. The calibration proceeds as follows. First, determine the median using the median detection block. Second, find the outliers in each row by first converting the analog current values from each cell and the median current to digital words. Next, calculate the absolute difference between the median value and the unit cell values and denote the two cells per row with the maximum absolute difference as the outliers. Following the outlier determination process, convert the summed row currents of the outlier-free DAC into digital words.

Median Detection

To determine the median current, we estimate the median value by comparing the current from the median cell (Fig. 2) with the current from each of the unit cells. The median cell is tuned to an output current such that the number of DAC unit cells with currents higher than the median cell’s is equal to the number of DAC unit cells with lower currents.

Fig. 2. Median detection circuit
Analog-to-Digital Conversion

For both the methods involved in the dual-calibration technique, we convert the analog current values into digital words and then calculate the difference from the median and the ranking of rows in digital domain as it is done in many of the switching-based calibration techniques. Low-resolution analog-to-digital conversion is performed using a 6-bit current starved ring oscillator-analog-to-digital converter (CSRO-ADC), as shown in Fig. 3.

Design of DAC Unit Cell

Once the outliers for each row of the DAC have been determined, this information is stored in the unit cells as a valid bit (VB). The proposed DAC cell is similar to a standard single-ended DAC cell except for the additional memory to store the VB, as shown in Fig. 8. The memory is a standard 6T static random access memory (SRAM), along with a separate readout switch.
Column Selection Decoder

The column decoder maps the column bits of the DAC via a binary-to-thermometer decoder, as shown in Fig. 4(a). Because of the redundant and invalid cells, the decoder also must consider the status stored in the memories of the cells in a row. If a cell is invalid, then it must be skipped by the decoder.

Row Selection Decoder

Due to the reordering of the rows, instead of a standard binary-to-thermometer decoder, a row selection decoder is used that consists of digital comparators and a memory bank of 16 4-bit SRAMs, where once the ranks of the rows have been determined, the order is stored. Each row rank is written sequentially, requiring 16 address cycles for this operation. For each row in the DAC, row selection decoder has two outputs—next Row and Row. During the DAC operation, the incoming row bits, rb are compared with the stored ranks using digital comparators, as shown.
in Fig. 4(b), to switch on the appropriate rows. For rows with rank > rb, Next Row is high and for rows with rank ≥ rb, Row is set high.

**Advantages:**

- Improve the static linearity
- Reduce the error

**Software implementation:**

- Tanner tools