EMDBAM: A Low-Power Dual Bit Associative Memory with Match Error and Mask Control

Abstract:

A ternary content addressable memory (TCAM) speeds up the search process in the memory by searching through prestored contents rather than addresses. The additional don’t care (X) state makes the TCAM suitable for many network applications but the large amount of cell requirement for storage consumes high power and takes a large design area. This paper presents a novel architecture of TCAM, which prestores 2 bits of data in an up–down manner and provides multiple masking operations through a single control multi-masking circuit. The proposed dual bit associative memory with match error and mask control (EMDBAM) consumes low power and selects the valid value on matchline through match error controller. The proposed design has been implemented using a standard 45-nm CMOS technology, and the extracted layout has been simulated using SPECTRE with the supply voltage at 1 V. The proposed EMDBAM can reduce the cell area by 39% compared with a basic TCAM design with a reduction of 9.6% in the energy delay product. The proposed architecture of this paper the area and power consumption are analysis using tanner tools.

Enhancement of the project:

Change the parameter and technology.

Existing System:

Chang et al. have segmented TCAM cells based on the mask bit values. The mask bits with only 1 value have been separated from those having only 0 values. Except the boundary cells, all other cells in different segments have been self-gated. Ruan et al. have partitioned the input bit stream into several groups; among these, the output has been derived with the use of a block XOR approach. A significant reduction in power consumption can be achieved, but it completely depends on the matching probability. The pre-computation circuitry takes a large area of design too. A logic-in-memory structure has been implemented to reduce the memory access time.
A magnetic tunnel junction/CMOS hybrid structure has been integrated with it for reducing leakage power consumption. The TCAM word MLs have been separated into four segments. The first segment has been pre-charged, and the rest have been charge-shared. Here, a mismatch in one segment does not drain the ML charge in the other segments. By using the dynamic power source technique, a mask data value has been used to destroy the pre-stored data. Scalability of TCAM has been improved with the exclusion of priority encoder. Using these architectures, leakage power consumption can be reduced significantly. Single-bit CAM cells have been arranged in the up–down approach (one with a stored value of 1 and the other with 0). As search bit contains only 0s or 1s, either upper or lower cell provides a match condition. A priority detector at the final stage ensures correct match output when a perfect match does not occur in both CAM cells. However, this does not give the functionality of a TCAM, which is an essential requirement in many network applications.
Fig. 1. Simplified functional block of the conventional TCAM.

All the non-segmented architectures have suffered from high leakage power consumption. The segmented architectures have resolved this issue, but the storage cell count remains the same. The conventional fully parallel TCAM presented in Fig. 1 consists of a data storage cell, a mask storage cell, and an evaluation logic that increases the physical size and interconnection wires [data wordline (WL) and mask WL].

**Disadvantages:**

- High leakage power consumption
Proposed System:

The DBAM has been designed using two CAMs (upper CAM and lower CAM) placed in an up–down approach, as shown in Fig. 2. The upper and lower CAMs have been pre-stored with alternate logic values (0 or 1) through (DL1 or DL1') and (DL2 or DL2'). Separated SL and SL from data lines have been provided to both CAMs. A mask storage cell has been placed for each DBAM, and the mask value of it (M or M') has been used for comparison with the match outputs of both upper and lower CAMs (FL1 and FL2). A common WL has been applied to both CAM cells as well as mask storage cell.

![High-level architecture of the proposed EMDBAM.](image)

The search values provided to the DBAM are either 0 or 1 at no mask condition, so it matches with one of the stored CAM values. The match function is similar to a conventional NAND-type.
TCAM shown in Fig. 3(a). For local masking, the value of a mask storage cell is set to 1, which provides a wild match to all search values. The SCMMC requires only one mask storage cell for the whole array of CAM blocks, as shown in Fig. 3(b). The SCMMC outputs (XL1 and XL2) and CAM MLs (FL1 and FL2) have been provided as inputs to the comparison circuit, as shown in Fig. 3(c). The masking of both upper and lower CAMs has been controlled by an SCMMC, as shown in Fig. 3(d).

MATCH ERROR CONTROLLER

The search values match either with upper or lower CAM cell values in most search conditions, but there are the possibilities of DMM, dual match (DM), and reverse match (RM) with the storage values. In these conditions, valid values must be passed to the MLs. For this purpose, we introduce the MEC as shown in Fig. 4(a) that comprises ECR, MBC, and PS. The ECR gives a match error when there is a change in the preset values.

Fig. 3. (a) Conventional NAND-type TCAM. (b) DBAM comprising 10T upper and lower CAMs with mask storage. (c) Comparison circuit. (d) SCMMC.

MATCHLINE SELECTION, SENSING, AND ADDRESS ENCODER SYSTEM

The MLS and the ML sense amplifier are shown in Fig. 4(b). In designs that use a basic TCAM structure, the ML is pre-charged to VDD at first. When a match occurs in all CAM cells in a row,
the ML is charged down to 0. However, in the proposed design, the MLs are not precharged rather controlled by the WL. A two stage selectors, as shown in Fig. 4(b), has been used for selecting the valid value (UML or PML or MML) to the ML. The first stage has been controlled by DMI and second by ER.

Fig. 4. (a) MEC includes three fundamental blocks: error checking circuit (ECR), MBC, and PS. U1 and U2 are unprocessed MLs of the previous slot. (b) Two stage MLS with modified charge-shared ML sense amplifier.

Advantages:

- reduce power consumption

Software implementation:

- Tanner tools