High-Speed and Energy-Efficient Carry Skip Adder
Operating Under a Wide Range of Supply Voltage Levels

Abstract:

In this paper, we present a carry skip adder (CSKA) structure that has a higher speed yet lower energy consumption compared with the conventional one. The speed enhancement is achieved by applying concatenation and incrimination schemes to improve the efficiency of the conventional CSKA (Conv-CSKA) structure. In addition, instead of utilizing multiplexer logic, the proposed structure makes use of NAND-NOR-Invert (NNI) and NOR-NAND-Invert (NNI) compound gates for the skip logic. The structure may be realized with both fixed stage size and variable stage size styles, wherein the latter further improves the speed and energy parameters of the adder. Finally, a hybrid variable latency extension of the proposed structure, which lowers the power consumption without considerably impacting the speed, is presented. This extension utilizes a modified parallel structure for increasing the slack time, and hence, enabling further voltage reduction. The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx 14.2.

Enhancement of the project:

Existing System:

adders are a key building block in arithmetic and logic units (ALUs) and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. There are many works on the subject of optimizing the speed and power of these units, which have been reported. Obviously, it is highly desirable to achieve higher speeds at low-power/energy consumptions, which is a challenge for the designers of general purpose processors. One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage.

Moreover, the subthreshold current, which is the main leakage component in OFF devices, has an exponential dependence on the supply voltage level through the drain-induced barrier lowering effect. Depending on the amount of the supply voltage reduction, the operation...
of ON devices may reside in the super threshold, near-threshold, or subthreshold regions. Working in the super threshold region provides us with lower delay and higher switching and leakage powers compared with the near/subthreshold regions. In the subthreshold region, the logic gate delay and leakage power exhibit exponential dependences on the supply and threshold voltages. Moreover, these voltages are (potentially) subject to process and environmental variations in the nano-scale technologies. The variations increase uncertainties in the aforesaid performance parameters. In addition, the small subthreshold current causes a large delay for the circuits operating in the subthreshold region.

CONVENTIONAL CARRY SKIP ADDER:

The structure of an N-bit Conv-CSKA, which is based on blocks of the RCA (RCA blocks), is shown in Fig. 1. In addition to the chain of FAs in each stage, there is carry skip logic. For an RCA that contains N cascaded FAs, the worst propagation delay of the summation of two N-bit numbers, A and B, belongs to the case where all the FAs are in the propagation mode. It means that the worst case delay belongs to the case where

\[ P_i = A_i \oplus B_i = 1 \text{ for } i = 1 \ldots N \]
Where $P_i$ is the propagation signal related to $A_i$ and $B_i$. This shows that the delay of the RCA is linearly related to $N$. In the case, where a group of cascaded FAs are in the propagate mode, the carry output of the chain is equal to the carry input. In the CSKA, the carry skip logic detects this situation, and makes the carry ready for the next stage without waiting for the operation of the FA chain to be completed. The skip operation is performed using the gates and the multiplexer shown in the figure. Based on this explanation, the NFAs of the CSKA are grouped in $Q$ stages. Each stage contains an RCA block with $M_j$ FAs ($j = 1... Q$) And skip logic. In each stage, the inputs of the multiplexer (skip logic) are the carry input of the stage and the carry output of its RCA block (FA chain). In addition, the product of the propagation signals ($P$) of the stage is used as the selector signal of the multiplexer.

Fixed Stage Size CSKA:

By assuming that each stage of the CSKA contains $M$ FAs, there are $Q = N/M$ stages where for the sake of simplicity, we assume $Q$ is an integer. The input signals of the $j$th multiplexer are the carry output of the FAs chain in the $j$th stage denoted by $C^0_j$, the carry output of the previous stage (carry input of the $j$th stage) denoted by $C^1_j$ (Fig. 1).

The critical path of the CSKA contains three parts: 1) the path of the FA chain of the first stage whose delay is equal to $M \times T_{CARRY}$; 2) the path of the intermediate carry skip multiplexer whose delay is equal to the $(Q-1) \times T_{MUX}$; and 3) the path of the FA chain in the last stage whose its delay is equal to the $(M-1) \times T_{CARRY} + T_{SUM}$.

Disadvantages:

- High power consumption
- High area coverage

Proposed System:

The structure is based on combining the concatenation and the incrementation schemes with the Conv-CSKA structure, and hence, is denoted by CI-CSKA. It provides us with the ability to use simpler carry skip logics. The logic replaces 2:1 multiplexers by NAND-NOR-Invert (NNI) / NOR-NAND-Invert (NNI) compound gates (Fig. 2). The gates, which consist of fewer transistors, have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer. Note that, in this structure, as the carry propagates through the skip logics, it
becomes complemented. Therefore, at the output of the skip logic of even stages, the complement of the carry is generated. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the conventional one. Note that while the power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the proposed CI-CSKA is a little more than that of the conventional one. This is due to the increase in the number of the gates, which imposes a higher wiring capacitance (in the noncritical paths).

The internal structure of the incrementation block, which contains a chain of half-adders (HAs), is shown in Fig. 3. The reason for using both AOI and OAI compound gates as the skip logics is the inverting functions of these gates in standard cell libraries.
Proposed Hybrid Variable Latency CSKA Structure:

The basic idea behind using VSS CSKA structures was based on almost balancing the delays of paths such that the delay of the critical path is minimized compared with that of the FSS structure. This deprives us from having the opportunity of using the slack time for the supply voltage scaling. To provide the variable latency feature for the VSS CSKA structure, we replace some of the middle stages in our proposed structure with a PPA modified in this paper. It should be noted that since the Conv-CSKA structure has a lower speed than that of the proposed one, in this section, we do not consider the conventional structure. The proposed hybrid variable latency CSKA structure is shown in Fig. 4 where an Mp-bit modified PPA is used for the pth stage (nucleus stage). Since the nucleus stage, which has the largest size (and delay) among the stages, is present in both SLP1 and SLP2, replacing it by the PPA reduces the delay of the longest off-critical paths. Thus, the use of the fast PPA helps increasing the available slack time in the variable latency structure. It should be mentioned that since the input bits of the PPA block are used in the predictor block, this block becomes parts of both SLP1 and SLP2.
In the proposed hybrid structure, the prefix network of the Brent–Kung adder is used for constructing the nucleus stage (Fig. 4). One the advantages of this adder compared with other prefix adders is that in this structure, using forward paths, the longest carry is calculated sooner compared with the intermediate carries, which are computed by backward paths. In addition, the fan-out of adder is less than other parallel adders, while the length of its wiring is smaller. Finally, it has a simple and regular layout.
Advantages:

- Reduce power consumption
- Reduce area coverage

Software implementation:

- Modelsim
The Master of IEEE Projects

- Xilinx ISE