Power Efficient Level Shifter for 16 nm FinFET near Threshold Circuits

Abstract:
Since the minimum feature size has shrunk beyond the sub-30-nm node, power density has become the major factor in modern microprocessors. Techniques such as dynamic voltage scaling operating down to near threshold voltage levels and supporting multiple voltage domains have become necessary to reduce dynamic as well as static power. A key component of these techniques is a level shifter that serves different voltage domains. This level shifter must be high speed and power efficient. The proposed level shifter translates voltages ranging from 250 to 790 mV, and exhibits 42% shorter delay, 45% lower energy consumption, and 48% lower static power dissipation. In addition, the proposed level shifter exhibits symmetric rise and fall transition times with up to 12% skew at the extreme conditions over the maximum range of voltages. The proposed architecture of this paper the area and power consumption are analysis using tanner tools.

Enhancement of the project:
Change the nanometer technology based on the power and area reduction.

Existing System:
Level shifter circuits are typically based on one of three approaches. One approach is based on a differential cascade voltage switch (DCVS) level shifter. This approach is discussed in this section to exemplify the basic principles used by the proposed level shifter. A second approach uses a Wilson current mirror in the amplifying stage. The third approach utilizes a specialized circuit topology.

Standard Level Shifter
A standard level shifter topology is typically based on a DCVS gate. A DCVS level shifter circuit is shown in Fig. 1. The input NMOS transistors are controlled by a low voltage input
signal, which is shifted to a high voltage at the output of the level shifter. The DCVS level shifter operates as follows. For the case when \(in=1\) (e.g., 250 mV) and \(in=0\) (e.g., 0 V), \(out=1\) (e.g., 790 mV) and \(out=0\) (e.g., 0 V). When the input transitions to \(in=0\) (e.g., 0 V) and \(in=1\) (e.g., 250 mV), the NR transistor enters the OFF state, while the NL transistor begins to conduct current, discharging node out. The gate of the PL PMOS transistor is, however, connected to node out, which remains at 0 V, maintaining PL on to resist the NL transistor by simultaneously charging node out. Note that the gate of NR and NL is connected to the low input signal.

These transistors operate near the cutoff region. The gate of PR and PL is connected to the high voltage supply. In this configuration, NL and NR struggle to sink more current than the PMOS pull-up transistors source. If NL sinks greater current than the PMOS pull-up transistor sources, node out discharges. The PR transistor toggles from the OFF state to the ON state, and charges node out (e.g., 790 mV), which cuts off the pull-up transistor PL, completing the transition.

Advanced Level Shifter

Fig. 1. Standard level shifter based on simple DCVS gate.
Additional logic is added to improve the performance and decrease the size of the NMOS pull-down transistors. The additional transistors are NRT, NLT, PRT, and PLT (Fig. 2). This circuit structure improves on the standard level shifter in two ways. First, the NMOS transistors NLT and NRT are biased at a nominal voltage (Vddh); NL and NR can, therefore, be smaller than a standard level shifter. NL and NR should, however, be sufficiently large to force the transition within the differential structure. When the differential input is sufficiently shifted, the significantly stronger NLT and NRT transistors complete the transition. Second, the PMOS transistors, PLT and PRT, are controlled with corresponding input voltage to limit the current flowing through the full voltage pull-up transistors, PL or PR. For high input in (in), PLT (PRT) is fully ON, providing the desired charging current, while PRT (PLT) limits the current, allowing the NR (NL) and NRT (NLT) NMOS pull-down network to discharge the out (out) node.

Fig. 2. Advanced level shifter based on DCVS gate with additional logic to improve speed

Disadvantages:

- Less sensitivity
Proposed System:

The proposed circuit dynamically changes the current sourced by the relevant PMOS pull-up transistor (PL/PR) to ensure that the weak NMOS pull-down transistor (NL/NR) sinks more current than the PMOS pull-up (PL/PR) network sources. The proposed low voltage level shifter is shown in Fig. 3.

Structure of the Proposed Wide Voltage Range Level Shifter: The novelty of this circuit topology is the feedback loop. The feedback loop consists of a delay element that connects the output node D (high voltage domain) to the input of two multiplexers, MUXL and MUXR. The delay element is based on two minimum sized serially connected inverters. These inverters are supplied with a high voltage (790 mV) and receive a high voltage signal D as an input. This delay element does not affect the delay of the proposed level shifter, since the delay element is within the feedback loop that sets up the circuit for the next transition. The MUXs are based on two sets of pass gates, as shown in Fig. 4. The output of MUXL (high voltage domain) is connected to the gate of the PMOS pull-up transistor PL. When select is high (high voltage domain), the gate of PL is connected to the intermediate voltage Vddm, which temporarily weakens PL. When select is low, the gate of PL is connected to node D, which preserves the differential operation. Similarly, the output of MUXR is connected to the gate of the PMOS pull-up transistor PR. When select is high, the gate of PR is connected to node D, which preserves the differential operation. When select is low, the gate of PR is connected to the intermediate voltage Vddm, which temporarily weakens PR.
(a)

(b)

c

LeMenizInfotech

36, 100 Feet Road, Natesan Nagar, Near Indira Gandhi Statue, Pondicherry-605 005.

Call: 0413-4205444, +91 9566355386, 99625 88976.

Web :www.lemenizinfotech.com/ www.ieemaster.com

Mail : projects@lemenizinfotech.com
Structure of the proposed wide voltage range level shifter, including (a) level shifter circuit, (b) internal MUX structures, and (c) intermediate voltage generator.

This configuration eliminates the need for the large NMOS pull-down transistors, NL and NR, because the relevant PMOS pull-up transistor is maintained at a low voltage bias for the upcoming transition. This approach also greatly lowers the transition time as compared with other level shifters.

The intermediate voltage Vddm is generated by a voltage divider, as shown in Fig. 3, which consists of five minimum sized diode connected PMOS transistors. In this configuration, a stable bias voltage of 450 mV is generated to weaken, as needed, the pull-up PMOS transistors.

Advantages:

- Increased sensitivity
- Speed increased
- Energy improved
- Power efficiency is increased

Software implementation:

- Tanner tools