Toward Solving Multichannel RF-SoC Integration Issues through Digital Fractional Division

Abstract:

In modern RF system on chips (SoCs), the digital content consumes up to 85% of the IC chip area. The recent push to integrate multiple RF-SoC cores is met with heavy resistance by the remaining RF/analog circuitry, which creates numerous strong aggressors and weak victims leading to RF performance degradation. A key such mechanism is injection pulling through parasitic coupling between various LC-tank oscillators as well as between them and strong transmitter (TX) outputs. Any static or dynamic frequency proximity between aggressors (i.e., oscillators and TX outputs) and victims (i.e., oscillators) that share the same die causes injection pulling, which produces unwanted spurs and/or modulation distortion. In this paper, we propose and demonstrate a new frequency planning technique of a multicore TX where each LC-tank oscillator is separated from other aggressors beyond its pulling range. This is done by breaking the integer harmonic frequency relationship of victims/aggressors within and between the RF transmission channels using digital fractional divider based on a phase rotation. Each oscillator’s center frequency can be fractionally separated by ∼28% but, at the same time, both producing closely spaced frequencies at the phase rotator outputs. The injection-pulling spurs are so far away that they are insignificantly small (−80 dBc) and coincide with the second harmonic of the carrier. This method is experimentally verified in a two-channel system in 65-nm digital CMOS, each channel comprising a high-swing class-C oscillator, frequency divider, and phase rotator. The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx 14.2.

Enhancement of the project:

Existing System:

As shown in Fig. 1, each oscillator and PA can couple resistively, magnetically, and capacitively to each other. In many cases, due to the low-resistivity substrate, which is the case for the scaled CMOS technology, noise/interference can pass throughout the entire chip. Thus, the analog
circuits nearby the noise/interference sources will suffer the most. Fig. 1 shows the aggressor/victim scenarios in the most recent multicore radios.

![Diagram of a two-core multiradio system and various pulling paths with aggressors and victims.](image)

There are well-known solutions attempting to reduce them. The most straightforward one is to reduce the coupling strength by increasing the physical distance between the strong aggressor and the sensitive victim and further isolating them with guard rings. Moreover, ground pickup connections can be used in between the two parts to absorb the interference. In addition, putting sensitive analog/RF parts in a deep N-well can be beneficial. These solutions, however, increase the chip fabrication cost, which is not desirable in high-volume consumer electronics.

**Fractional Divider**

The injection pulling has been traditionally mitigated by operating the oscillator at integer multiples of the output RF carrier. Unfortunately, that arrangement does not entirely eliminate the pulling since the PA harmonics still coincide with the oscillator center frequency.

**Frequency Planning**
In this paper, we propose a digital fractional divider architecture suitable for the pulling-free frequency planning scheme for multichannel TXs. Fig. 2(top) shows the scenario in which the two oscillators operate at almost the same frequency.1 Since the coupling strength is high, it leads to high spurious content in the spectrum of both oscillators. If two oscillators’ center frequencies are separated, as per (2), the coupling effects will decrease, as shown in Fig. 7(bottom). Since the output frequencies of the two channels need to be the same (on average), a noninteger (fractional) type divider should be used afterward.
Fig. 3. Different frequency planning scenarios for multichannel pulling mitigation through digital dividers with an output frequency of about 2 GHz (e.g., coexistence of Bluetooth and WiFi). (a) Integer divide by 2. (b) Integer divide by 4. (c) Fractional divide by 2.5 and 1.5. (d) Fractional divide by 3.5 and 4.5.

Employing a fractional frequency divider, as shown in Fig. 3, is the proposed method here to prevent both direct and harmonic PA pulling within and between the channels. The reason for using an eight-phase rotation (÷4 and then phase rotator) is as follows: the integer ÷2 in Fig. 3(a) has a disadvantage of two oscillators operating at the same frequency, causing their strong mutual pulling. The second harmonic of the PA can also pull both oscillators.

Disadvantages:

- Low speed

Proposed System:

In this paper, we propose a low-power architectural solution that avoids the pulling problem altogether through a large fractional frequency translation of both the aggressor and victim circuits. Although this research specifically targets cellular base station TXs, the findings are applicable to cellular mobile applications, especially multicore RF-SoCs. Hence, the emphasis is on low phase-noise implementation. Fig. 4 contains two oscillators, each with an edge rotator.
This corresponds to the two-channel system of Fig. 1. The frequency translation direction depends on the edge rotation direction. The frequencies of the two channel outputs (OUT1 and OUT2) are the same \( f_{o1} = f_{o2} = f_{TX} \), or very close to each other due to the modulation, but the center frequencies of the oscillators \( f_{osc1} \) and \( f_{osc2} \) are well separated.

![System-level block diagram and circuit details of the phase rotator are shown in Fig. 5(a).](image)

System-level block diagram and circuit details of the phase rotator are shown in Fig. 5(a). The rail-to-rail CMOS \( \div 4 \) divider [see Fig. 5(b)] generates eight equidistant phases. Out of four different configurations, Fig. 5(b) (1) divider topology was chosen for its better noise performance and shorter propagation delay. Adding back-to-back inverters improves delay matching at the cost of small degradation in the phase noise. The rotating system contains a ring counter with set/reset to control the normal pass through or the fractional division (see Fig. 5). When set is asserted, only one of the mux select signals will be active and it operates as a normal \( \div 4 \). If reset is deasserted, logic 1 circulates in the ring counter and generates the proper selection signal.
To guarantee this, consideration of the worst case timing uncertainty is needed. The critical timing delay [see Fig. 5(a)] mainly comprises CLK-to-Q in the ring counter and CLK-to-Q delay for the retimer with enough setup time to have reliable selection in different process corners. In order to relax the timing, an edge-triggered flip-flop was chosen that exhibits small setup and hold times. Taking into account these delays results in choosing the appropriate signal phase (P1–P8) to retime the counter output to generate correct select signals for the multiplexer (S1–S8).

Advantages:

- Increase the speed

Software implementation:

- Modelsim
- Xilinx ISE