Ultralow-Energy Variation-Aware Design: Adder Architecture Study

Abstract:

Power consumption of digital systems is an important issue in nanoscale technologies and growth of process variation makes the problem more challenging. In this brief, we have analyzed the latency, energy consumption, and effects of process variation on different structures with respect to the design structure and logic depth to propose architectures with higher throughput, lower energy consumption, and smaller performance loss caused by process variation in application specific integrated circuit design. We have exploited adders as different implementations of a processing unit, and propose architectural guidelines for finer technologies in subthreshold which are applicable to any other architecture. The results show that smaller computing building blocks have better energy efficiency and less performance degradation because of variation effects. In contrast, their computation throughput will be mid or less unless proper solutions, such as pipelined or parallel structures, are used. Therefore, our proposed solution to improve the throughput loss while reducing sensitivity to process variations is using simpler elements in deep pipelined designs or massively parallel structures. The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx 14.2.

Enhancement of the project:

Existing System:

The SSTA is an accepted method based on statistical manner of variations and supported by recent commercial tools. In this method, $\sigma / \mu$ is an important ratio to compare the severity of variations in cells to have better standard cell design in deep subthreshold region. Verma et al. extracted logic chains for Kogge–Stone adder (KSA) to measure delay variability in both 0.3 and 1.2 V voltages. $\sigma / \mu$ ratio contours have been drawn based on delay variability histogram, logic depth, and gate width, and variability mitigation is performed by gate up-sizing. Newer technologies such as dual gate silicon on insulator have lower variability in comparison with bulk CMOS to design robust subthreshold logic cells in 32-nm CMOS.
Thakur et al. analyzed the effects of variations in gate oxide thickness, supply voltage, and temperature in four adders and they tried to rank the variation effect of each parameter on delay. As a new design method, SSTA is used to sieve a standard cell library with different variation constraints during synthesis of arithmetic circuits. They have verified the results by Monte Carlo simulations. Islam et al. have designed a robust (lower σ/μ ratio) subthreshold full adder considering power-delay product. Arthurs and Di evaluate the variations of both Schmitt-trigger and NULL convention logic 1-bit adders by four-gate libraries characterized at different supply voltages for better static noise margin.

Disadvantages:

- Area and power are high

Proposed System:

We choose adder as the key building block of arithmetic units in every processor ranging from general purpose to application specific, because it can be used to implement more complex operations such as multiplication and division or even more complex units, such as fast Fourier transform and finite-impulse response filters. We have selected six different 16-bit adder structures to study in subthreshold region.

Ripple-carry adder (RCA) has simple architecture and linearly extensible for wider computations with respect to area. However, this adder has limited performance because of long carry propagation path from LSB to MSB. Because of long critical path delays in RCA, designers have tried to look ahead carry bit for each higher bit independent of lower neighboring carry bits using a logarithmic delay tree structure, and each tree optimization strategy implies a new prefix adder.

The first candidate prefix adder discussed is Brent–Kung adder (BKA). This structure has balanced area and timing overheads with shortening the long carry chains \(((2\times \log_2 N) − 2)\) logic stages\] which is a proper technique to co-optimize area and performance of design. In KSA, addition is performed with higher speed because of parallel computations in shorter paths with only \(\log_2 N\) logic stages besides higher area overhead. Han–Carlson adder (HCA) is a combination of BKA and KSA to reduce the complexity and make a tradeoff between area and delay with \(\log_2 N + 1\) logic stages. Another prefix adder which has minimum logic depth (\(\log_2 N\)) is known as Lander–Fisher adder (LFA). In this architecture, some nodes have very high fan-outs (up to \(N/2\)) to reduce the area and this may degrade the performance. Serial full adder (SFA)
is a basic full adder which is combined with a flip-flop to utilize the adder unit at different clock cycles in time-serialized ripple-carry manner (Fig. 1) and the number of clock cycles that it takes is equal to the number of bits.

Advantages:

- Area and power are low

Software implementation:

- Modelsim
- Xilinx ISE