Understanding the Relation between the Performance and Reliability of NAND Flash/SCM Hybrid Solid-State Drive

Abstract:

A NAND flash memory/storage-class memory (SCM) hybrid solid-state drive (SSD) can achieve higher performance than the conventional NAND flash-only SSD. Error-correcting codes (ECCs) are applied to the SSD to correct bit errors occurring inside the NAND flash and SCM. To correct more bit errors, the stronger ECC is required and the ECC latency increases. This paper evaluates the relation between the performance and the reliability of the NAND flash/SCM hybrid SSD. First, how the ECC latency impacts the SSD performance is analyzed. Then, the SSD performances are evaluated with various data-access patterns. The ECC effect is significantly different among the data access patterns. Moreover, four scenarios of the SCM reliability are established and the performances are evaluated with the four data-access patterns. When the SCM reliability becomes high, the decrease in the throughput due to the ECC for SCM becomes significantly small. Finally, by setting the acceptable SSD performance, the acceptable bit-error rate (BER) of the SCM is evaluated. The SCM BER can be as high as around 0.9%. The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx 14.2.

Enhancement of the project:

Existing System:

As NAND flash memory cost per bit declines, its capacity and density increase and endurance improves, NAND flash solid-state disks (SSD) are becoming a viable data storage solution for portable computer systems. Their high performance, low power and shock resistance provide an alternative to hard disk drives (HDD).

SSD vs. HDD: NAND flash memory capacity has been doubling every year as Hwang’s rule suggests. Migration to lower processing nodes and development of multi-level (MLC) cell
technology have been driving its bit cost lower while improving its endurance and write performance. Therefore solid-state disks are becoming an attractive replacement for conventional hard disks.

There are number of reviews available online each of which compares the performance of an SSD against an HDD using various applications as benchmarks. For example; a sample 64 GB SSD with SATA 3 Gb/s interface performs 9 times faster in loading applications (e.g., loading office work, outlook, internet explorer, adobe Photoshop) compared to various 7K and 10K RPM hard disks. Another popular benchmark is startup time for Windows Vista. In this benchmark, performance of a solid-state disk is reported to be 3 times better than conventional magnetic disks. In order to better understand the performance difference between conventional hard disks and solid-state disks, we need to take a closer look into how an I/O request is serviced in both systems.

Typical characteristics of I/O traffic in personal computers can be described as bursty, localized in areas of the disk and partitioned 50:50 between reads and writes. Average I/O request size is 7-9 KB and I/O traffic load is estimated to be around 2.4 Mbits per second. We can consider an 8 KB request as a benchmark point and estimate the average request service for a read and a write request.
Fig. 1. Schematic of a NAND flash block.

The main different features between the NAND flash memory and SCM from the viewpoint of the SSD performance are the read/write latencies, write data-unit size, and in-place overwrite capability. Since the write latency is large [around 1 ms, many cells of the NAND flash memory are simultaneously programmed to improve the write throughput. The write unit of the NAND flash is called a page that contains typically 16 kB. Fig. 1 defines the page and the block of the multilevel cell (MLC) NAND flash with a multipage-cell architecture. The multipage-cell architecture improves the program/read performance. Each bit in a cell is classified into lower and upper pages. The lower page is first programmed by splitting the memory cell VTH into two memory states. Then, the upper page is programmed and the memory cells are allocated to one of the four memory states. The programming and reading by the multipage-cell architecture are in average 1.5 times faster than just simultaneously programming/reading both upper and lower pages, because the number of programming/reading steps is reduced.

Disadvantages:

- Reliability is less

Proposed System:

In contrast to the NAND flash-only SSD, new data are either written to the NAND flash memory or the SCM, based on the data size. When the data are written to the NAND flash memory, if the LBA points a clean page, only the ECC encoding is required and the ECC latency is negligibly small. When the data are written to the SCM, since sector unit (over)writing is accepted, the data can be written without reading the old data.

Two operations specific to the hybrid SSD is described below. First, reconsider-as-a-fragment migrates the hot/random data from the NAND flash to SCM. Since the data are read from the NAND flash, the ECC decoding latency for the NAND flash (tECC_NAND) should be considered. Second, a cold data eviction (CDE) algorithm transfers the cold/sequential data from the SCM to the NAND flash when the free space of the SCM decreases [19]. The SCM is read during the CDE with ECC decoding latency for SCM (tECC_SCM). Moreover, also in the NAND flash/SCM hybrid SSD, the garbage collection is executed.
Impact of ECC on NAND Flash Read Time

Fig. 2 explains how the ECC decoding latency (t_{ECC}) impacts the read performance. Note that to estimate the lower bound of the ECC performance, the pipeline operation of the syndrome calculation, BM, and Chien search inside the ECC decoder is not considered. Although Fig. 2 shows the examples with NAND flash memories, t_{ECC} for the SCM can be discussed similarly. Basically, the impact can be analyzed based on the four classifications: random/sequential read with short/long t_{ECC}.

Impact of ECC on the SSD Write Performance
The effect of the increase in the total read time due to the ECC is translated to the SSD write performance. Read operations are invoked during write accesses and the ECC latency decreases the write throughput.

Advantages:

- Improve the reliability
- Improve the performance

Software implementation:

- Modelsim
- Xilinx ISE