Unequal-Error-Protection Error Correction Codes for the Embedded Memories in Digital Signal Processors

Abstract:
In many digital signal processing applications, some parts of a word stored in the embedded static random access memories (SRAMs) are more important than other parts of the word. Due to the differences in importance, memory failures that occur in more important bit locations generally give rise to relatively larger system performance degradation than those in less important locations. This brief presents a low-complexity unequal-error-protection error correcting code (UEEP-ECC) approach for the embedded memories in digital signal processor. In the proposed UEEP-ECC, repetition code is combined with the Bose–Chaudhuri–Hocquenghem code to selectively provide stronger error correction capabilities on more important data portions without a large hardware overhead. An efficient UEEP-ECC generation algorithm that can find the UEEP-ECC code with a minimum power of memory core and ECC logics is also presented. The experimental results show that the UEEP-ECC scheme achieves considerable power savings and data quality improvements in both of the H.264 and fast Fourier transform applications. The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx 14.2.

Enhancement of the project:
Furthermore reduction in power and area of the architecture.

Existing System:
One of the fundamental problems encountered with the conventional uniform ECC approaches is that the ECC protection is equally applied to all memory blocks without considering the differences in importance among the data in a word of embedded memory. However, in many applications, some parts of the data in a word are much more important than other parts. For example, in the embedded memory of digital signal processor (DSP), the failures in the memory bit-cells storing high-order bits (HOBs), which are also called the most significant bits, give rise to much larger output quality degradation than those of the low-order bits (LOBs). Considering the differences in importance in memory, modified ECC ideas have been proposed to strongly
protect the HOB data bits in the embedded SRAM memories of the DSPs. Although considering the differences in importance in memory, modified ECC ideas have been proposed to strongly protect the HOB data bits in the embedded SRAM memories of the DSPs. Although the tradeoff between the error correction performance and area overhead is considered in the approaches, since the ECC schemes are focused on low-latency decoding, area overhead due to large parity bits and increasing decoder complexity are still very expensive.

This brief presents a novel low-complexity and low-latency unequal-error-protection ECC (UEEP-ECC) for the embedded SRAM memories inside the DSPs. In the proposed ECC scheme, by efficiently merging repetition code over the Bose–Chaudhuri–Hocquenghem (BCH) code, the UEEP-ECC offers stronger error corrections on HOB parts without large area overhead due to parity bits and decoder complexity. An efficient ECC generation algorithm with low area and low-latency hardware architecture is also presented to achieve the minimum power consumption of memory core and ECC encoder/decoder.

SRAM Reliability Degradation with Supply Voltage Scaling:

In the SRAM bit-cells, possible failures under process variations can be broadly categorized as delay and functional failures. Since many dedicated DSP applications, such as H.264 and fast Fourier transform (FFT) processors, often allow low operation frequency, the delay constraint can be easily satisfied using the 65-nm technology even with supply voltage scaling. In low voltage operation with process variations, the SRAM bit-cell arrays still suffer from functional failures due to negative read static noise margin and negative write margin. Under process variations, the worst process corners for read and write operations are fast-nMOS and slow-pMOS (FS) and slow-nMOS and fast-pMOS (SF) corners, respectively.

Disadvantages:

• System performance degradation is high

Proposed System:

Fig. 1 shows a brief concept of the proposed UEEP-ECC code decoding procedure. Since the decoding of the repetition code in the HOB part can be simply implemented using majority voting modules without latency overhead, the repetition code can be easily merged into the BCH decoding process without incurring additional latency. Since repetition code does not incur
additional errors even when it fails to correct the errors, BCH decoding can be processed over the decoded data (by repetition decoder) to correct the remaining errors.

Optimal UEEP-ECC Searching Algorithm

![Decoding procedure of the proposed UEEP code.](image)

In the proposed UEEP-ECC code selection algorithm, we will search for the UEEP-ECC that minimizes the power consumption of the memory core and ECC encoder/decoder while satisfying the system performance (MSE) constraint. Since multiple data are stored in a same word of memory in many DSP applications, let us assume that M data blocks are stored in a single word of memory.

Problem Definition: For a given target MSEtarget, data length m, memory size A (number of addresses), and M data blocks (each data block of m bits) stored in a word of SRAM, the proposed algorithm finds the supply voltage of memory, Vddopt, the error correction capabilities of BCH code (tBCH), the error correction capabilities of repetition codes for HOB bits to minimize the total power consumption including memory core, and ECC encoder/decoder while satisfying the given system performance (MSE) constraint.

Optimum UEEP Code Search Algorithm:

The main steps of the algorithm are described as follows.
1) Considering the data block of m bits and M data blocks stored in a word of SRAM, the initial degree of Galois field extension is determined for the BCH code.

2) Set the maximum error correction capability of BCH, t_{BCH}, max, as log2 (m × M). For each value of t_{BCH} from 0 to t_{BCH} max, do the following.
   a) When BCH with t_{BCH} cannot be implemented within GF (2^n), the degree of Galois field extension, n_{BCH}, is updated, and finds the parity bit-length of BCH (r_{BCH}).
   b) For each value of t_{REP}, sum from 0 to m, memory area (mem_{area}) is obtained with the (M · m + r_{BCH} + 2 · M · t_{REP}, sum) multiplied by the number of memory address A.
   c) For each value of t_{BCH} and t_{REP}, sum, one UEEP-ECC code set is selected among all the possible UEEP-ECC code sets as {(M · m, t_{BCH}), (h, t_{REP}) 1,...,(h, t_{REP})M }.
   d) For each of UEEP-ECC code set, from the initial supply voltage (Vdd) of 1.1 V, Vdd is scaled down with a step of 25 mV to find the Vddopt. At each level of Vdd, the algorithm calculates MSE and checks if they obtained MSE is smaller than the constraint MSE target. It also calculates the total power consumption including memory and ECC encoder/decoder using table lookup. If the power is smaller than power_{min} while satisfying the MSE target constraint, power_{min} is updated.

Proposed Low-Complexity UEEP-ECC Decoder Architecture

Compared with the conventional BCH decoder architecture, the two main modifications in the UEEP-ECC decoder are:
   1) combined syndrome calculation module for removing latency overheads of repetition code decoder and
   2) The modified majority voting decoder and Chien search (CS) module for reducing the decoder errors on the HOB parts.

As illustrated in Fig. 2(a) and (b), the combined syndrome calculation module performs syndrome calculation early without HOB parts in parallel with the repetition code decoding, and the outputs of the repetition decoder are fed into the BCH decoder for generating the total syndrome value.
UEEP-ECC Applied to the Embedded Memories of H.264 Encoder

The H.264 encoder compresses video data by using the spatial and temporal redundancies existing within and between the video frames. In order to measure the effect of the memory failures on the video quality degradation in the H.264 system, first, extensive Monte Carlo simulations are performed under various supply voltages, and the failure probabilities of SRAM...
bit-cells are obtained. Using the failure probabilities, the H.264 encoding simulations are performed with the JM reference tool.

For each memory word of the H.264 processor, it is assumed that one computational block size is 4 × 4 pixels. Since one pixel consists of 8 bits, 4 pixel data blocks (32 bits) are stored in a single word of the embedded memory. In our simulations, the SRAM failures are equally distributed within the memories of the H.264 encoder, and the video quality degradation is measured in the H.264 decoder side. As a measure of video quality, peak signal-to-noise ratio (PSNR) is used, this is a direct function of the MSE metric. With the given PSNR constraint of 30 dB, using offline simulations.

Advantages:

- System performance degradation reduced

Software implementation:

- Modelsim
- Xilinx ISE