A High-Speed and Power-Efficient Voltage Level Shifter for Dual-Supply Applications

Abstract:

This brief presents a fast and power-efficient voltage level shifting circuit capable of converting extremely low levels of input voltages into high output voltage levels. The efficiency of the proposed circuit is due to the fact that not only the strength of the pull-up device is significantly reduced when the pull-down device is pulling down the output node, but the strength of the pull-down device is also increased using a low-power auxiliary circuit. Post layout simulation results of the proposed circuit in a 0.18-µm technology demonstrate a total energy per transition of 157 fJ, a static power dissipation of 0.3 nW, and a propagation delay of 30 ns for input frequency of 1 MHz, low supply voltage level of VDDL=0.4V, and high supply voltage level of VDDH=1.8V. The proposed architecture of this paper analyses the logic size, area and power consumption using Tanner tool.

Existing System:

One of the conventional level-shifting architectures is shown in Fig. 1(a). The operation of this circuit is as follows. When the input signal IN is “High=VDDL,” MN1 and MN2 are ON and OFF, respectively. Therefore, MN1 tries to pull the node Q1 down. Consequently, MP2 is gradually turned on to pull the node Q2 up to VDDH and to turn MP1 off. Similarly, when the input signal is changed to “Low=VSS,” the operation is forced to reverse states. It is noticeable that, in this structure, there is a contention at the nodes Q1 and Q2 between the pull-up devices (i.e., MP1 and MP2) driven with VDDH and the pull-down devices (i.e., MN1 and MN2) driven with VDDL. As a result, when the voltage difference between VDDL and VDDH is high and particularly when the input voltage is in subthreshold range, this circuit will no longer be able to convert the voltage levels. This is because the currents of the pull-down transistors are smaller than those of the pull-up devices.
To solve this problem, several attempts have been reported. One approach is to exploit technology-based strategies, e.g., employing strong pull-down devices using low-Vth transistors and/or weak pull-up networks by using high-Vth transistors. Another approach is to use strong pull-down devices by enlarging their width, leading to an increase in both the delay and the power consumption. The last solution is to reduce the strength of the pull-up device when the pull-down device is pulling down the output node. The structure illustrated in Fig. 1(b) uses a semi-static current mirror to limit the current and therefore the strength of the pull-up device (i.e., MP2) when the pull-down device is pulling down the output node. However, this structure suffers from the static current flowing through MN1 and MP1 during the “High” logic levels of the input signal. In order to decrease the static power consumption, a dynamic current generator, which turns on only during the transition times, can be used. The structure shown in Fig. 1(c) employs a dynamic current generator implemented by MP3. In this circuit, when the input signal IN goes from “Low” to “High,” MN2 turns off and MN1 turns on and pulls the node QB down. Since the node OUT had been “Low” (before the transition), during the time interval in which OUT is not corresponding to the logic level of the input signal IN, MP3 will be turned on. Therefore, a transition current flows through MN1, MP3, and MP1. This current is mirrored to MP2 (i.e., IP2) leading to pull the node OUT up. Finally, when OUT is pulled up to VDDH, MP3 is turned off and therefore no static current flows through MN1, MP3, and MP1. On the other hand, when the input signal IN is changed from “High” to “Low,” MN1 turns off and MN2 turns on trying to pull the node OUT down.
node\text{OUT} down. As the node\text{OUT} is gradually pulled down, MP3 is turned on trying to charge the node QB, which is already discharged to the ground, meaning that a transition current (i.e., IP1) flows through MP1 and MP3 to charge node QB. This current is mirrored to MP2 (i.e., IP2) and therefore tries to pull the node\text{OUT} up, while MN2 is trying to pull this node down. This means that there is still a contention between the pull-up and the pull-down devices in the high-to-low transition of the input signal, leading to increase in the delay and consequently the power consumption of the circuit, especially the power of the next stage.

Disadvantages:

- Power consumption is high

Proposed System:

In order to reduce the existing contention at the high-to-low transition of the structure shown in Fig. 1(c), the transition current of IP1 and therefore IP2 must be suppressed when MN2 is pulling down the output node. For this purpose, the structures shown in Fig. 2 is proposed. The operation of the proposed circuit, shown in Fig. 2(a), is as follows. When the input signal changes from "Low" to "High," MN1 is turned on and MN4 is turned off. During the transition time in which \text{OUT} is not corresponding to the logic level of the input, MN4 will be turned on, because the overdrive voltage of MP3 (i.e., V_{DDH}) is larger than that of MN3 (i.e., V_{DDL}). Therefore, a transition current flows through MN4, MN1, and MP1 (i.e., IP1). This current is mirrored into MP2 (i.e., IP2) and tries to pull up the output node. Finally, when \text{OUT} is pulled up, MP3 is turned off and consequently the gate of MN4 is pulled down by MN3 meaning that no static current flows through MN4, MN1, and MP1. It should be noted that in order to minimize the power consumption, the aspect ratio of MP1 is chosen smaller than that of MP2. As for the high-to-low transition of the input signal, MN2 is turned on trying to pull down the output node. At the same time, MN1 is turned off meaning that, in contrast to the structures shown in Fig. 1(c), roughly no transition current flows through MP1 (i.e., IP1 \approx 0) reducing the strength of MP2 when MN2 is pulling down the output node. However, it should be noted that the node QA is pulled up just to V_{DDH} - |V_{th}|, where V_{th} is the threshold voltage of MP1. This means that the current of MP2 (i.e., IP2) is not completely close to zero and consequently a weak contention still exists.
In order to further reduce the value of \(IP_2\), another device, i.e., MP4 in Fig. 2(a) is used. For more details, when \(MN_2\) is pulling down the output node, the gate of MP4 is “High” with the value of \(V_{DDL}\) and therefore the drain–source voltage of MP2 is decreased. As a result, as shown in Fig. 3, the propagation delay and therefore the power dissipation of the circuit will be decreased. It should be noted that if the gates of \(MN_2\) and MP4 are driven with a voltage higher than \(V_{DDL}\), not only the current of the pull-up device (i.e., \(IP_2\)) is drastically reduced, but also the strength of the pull-down device (i.e., \(MN_2\)) is increased. Thus, the contention and therefore the delay and the power (especially the power consumption of the next stage) are significantly reduced. Moreover, the level shifter will be able to operate correctly even for subthreshold input voltages. In order to apply this technique to the proposed structure, as shown in Fig. 2(b), an auxiliary circuit (i.e., MP5, MP6, MP7, MN5, MN6, and MN7) is used. This auxiliary circuit turns on only in the high-to-low transition of the input signal to pull up the node QC to a value larger than \(V_{DDL}\). The operation of this part of the circuit is as follows. When \(IN\) changes from “High” to “Low” and \(OUT\) is not still corresponding to the input logic level, \(MN_6\), \(MN_7\), and \(MP_6\) are turned on and \(MN_5\) is turned off. Therefore, a transition current flows through \(MN_6\), \(MN_7\), \(MP_6\), and mirrors to \(MP_7\) (i.e., \(IP_7\)) pulling up the node QC.

Advantages:

- Power consumption is reduced
Do Your Projects With Technology Experts…

Software implementation:

- Tanner tool