Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers

Abstract:

In this paper, we propose four 4:2 compressors, which have the flexibility of switching between the exact and approximate operating modes. In the approximate mode, these dual-quality compressors provide higher speeds and lower power consumptions at the cost of lower accuracy. Each of these compressors has its own level of accuracy in the approximate mode as well as different delays and power dissipations in the approximate and exact modes. Using these compressors in the structures of parallel multipliers provides configurable multipliers whose accuracies (as well as their powers and speeds) may change dynamically during the runtime. The efficiencies of these compressors in a 32-bit Dadda multiplier are evaluated in a 45-nm standard CMOS technology by comparing their parameters with those of the state-of-the-art approximate multipliers. The results of comparison indicate, on average, 46% and 68% lower delay and power consumption in the approximate mode. Also, the effectiveness of these compressors is assessed in some image processing applications. The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx 14.2.

Existing System:

While there are many works in designing approximate multipliers, the research efforts on accuracy configurable approximate multipliers are limited. In this section, we review some of these works. In [10], a static segment method (SSM) is presented, which performs the multiplication operation on an m-bit segment starting from the leading 1 bit of the input operands where m is equal to or greater than n/2. Hence, an m×m multiplier consumes much less energy than an n×n multiplier. Also, a dynamic range unbiased multiplier (DRUM) multiplier, which selects a nm-bit segment, starting from the leading 1 bit of the input operands, and sets the least significant bit of the truncated values to “1,” has been proposed. In this structure, the truncated values are multiplied and shifted to the left to generate the final output. Although, by exploiting smaller values form, the structure provides higher accuracy designs than those, its approach requires utilizing extra complex circuitry.
A bio inspired approximate multiplier, called broken array multiplier, has been proposed. In this structure, some carry save adder cells, in both vertical and horizontal directions during the summation of the partial products, have been omitted to save the power and area and reduce the delay. Two approximate 4:2 compressors have been proposed and utilized in Dadda multiplier. The proposed compressors only operated in the approximate mode. By modifying the Karnaugh map of a 2×2 multiplier (omitting one term in the Karnaugh map), an approximate 2×2 multiplier with a simpler structure has been proposed. This block may be used for constructing larger multipliers. Also, in this paper, an error detection and correction (EDC) circuit has been proposed. An inaccurate multiplier design strategy based on redesigning the multiplier into two multiplication and non-multiplication parts was introduced. The multiplication part was constructed based on the conventional multipliers while then on-multiplication part was implemented in an approximate structure with a specified value of error. It should be noted that both of the approaches presented suffer from high relative errors.

**Figure 1**: Block diagram of 4:2 compressor.

**Figure 2**: Structure of the conventional 4:2 compressor.
A high accuracy approximate 4×4 Wallace tree multiplier was proposed. This multiplier employed a 4:2 approximate counter leading to delay and power reductions of the partial product stage of the 4×4 Wallace tree. In this paper, the proposed small multiplier was used to form larger multipliers. Due to the array structure of this approximate multiplier, its delay was large. In addition, an EDC unit was suggested to be used at the output of the approximate 4 ×4 Wallace tree. The unit generated the exact output in the case of the exact operating mode. By proposing an approximate adder with a small carry propagation delay, the partial product reduction stage was sped up. In this paper, an OR-gate-based error reduction unit was also proposed. A rounding based approximate multiplier (ROBA) has been proposed that round the input operands into the nearest exponent of two. This way the multiplication operation became simpler. It should be noticed that the error recovery unit increases the power consumption and delay of the multiplier. This implies that accuracy configurable multipliers would have large delay and power overheads.

Exact 4:2 Compressor:

To reduce the delay of the partial product summation stage of parallel multipliers, 4:2 and 5:2 compressors are widely employed. The focus of this paper is on approximate 4:2 compressors. First, some background on the exact 4:2 compressor is presented. This type of compressor, shown schematically in Fig. 1, has four inputs (x1–x4) along with an input carry (Cin), and two outputs (sum and carry) along with an output Cout.

The internal structure of an exact 4:2 compressor is composed of two serially connected full adders, as shown in Fig. 2. In this structure, the weights of all the inputs and the sum output are the same whereas the weights of the carry and Cout outputs are one binary bit position higher. The outputs sum, carry, and Cout are obtained from

\[
\text{sum} = x_1 \oplus x_2 \oplus x_3 \oplus x_4 \oplus \text{Cin} \quad (1)
\]

\[
\text{carry} = (x_1 \oplus x_2 \oplus x_3 x_4) \text{Cin} + (x_1 \oplus x_2 \oplus x_3 \oplus x_4)'x_4 \quad (2)
\]

\[
\text{Cout} = (x_1 \oplus x_2)x_3 + (x_1 \oplus x_2)'x_1 \quad (3)
\]

Disadvantages:

- Delay is high
- Power consumption is high
Proposed System:

We present four dual-quality reconfigurable approximate 4:2 compressors, which provide the ability of switching between the exact and approximate operating modes during the runtime. The compressors may be utilized in the architectures of dynamic quality configurable parallel multipliers. The basic structures of the proposed compressors consist of two parts of approximate and supplementary. In the approximate mode, only the approximate part is active whereas in the exact operating mode, the supplementary part along with some components of the approximate part is invoked.

Proposed Dual-Quality 4:2 Compressors:

The proposed DQ4:2Cs operate in two accuracy modes of approximate and exact. The general block diagram of the compressors is shown in Fig. 3. The diagram consists of two main parts of approximate and supplementary. During the approximate mode, only the approximate part is exploited while the supplementary part is power gated. During the exact operating mode, the supplementary and some parts of the approximate parts are utilized. In the proposed structure, to reduce the power consumption and area, most of the components of the approximate part are also used during the exact operating mode. We use the power gating technique to turn OFF the unused components of the approximate part. Also note that, as is evident from Fig. 3, in the exact operating mode, tri-state buffers are utilized to disconnect the outputs of the approximate part from the primary outputs.

Figure 3: Block diagram of the proposed approximate 4:2 compressors. The hachured box in the approximate part indicates the components, which are not shared between this and supplementary parts.
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1) Structure 1 (DQ4:2C1): For the approximate part of the first proposed DQ4:2C structure, as shown in Fig. 4(a), the approximate output carry (i.e., carry’=x4) is directly connected to the input x4(carry’=x4), and also, in a similar approach, the approximate output sum (i.e., sum’=x1). In the approximate part of this structure, the output Cout is ignored. While the approximate part of this structure is considerably fast and low power, its error rate is large (62.5%).

![](image)

(a) Approximate part and (b) overall structure of DQ4:2C1

The supplementary part of this structure is an exact 4:2 compressor. The overall structure of the proposed structure is shown in Fig. 4(b). In the exact operating mode, the delay of this structure is about the same as that of the exact 4:2 compressor.

2) Structure 2 (DQ4:2C2): In the first structure, while ignoring Cout simplified the internal structure of the reduction stage of the multiplication, its error was large. In the second structure, compared with the DQ4:2C1, the output Cout is generated by connecting it directly to the input x3 in the approximate part. Fig. 5 shows the internal structure of the approximate part and the overall structure of DQ4:2C2. While the error rate of this structure is the same as that of DQ4:2C1, namely, 62.5%, its relative error is lower.
3) Structure3(DQ4:2C3): The previous structures, in the approximate operating mode, had maximum power and delay reductions compared with those of the exact compressor. In some applications, however, a higher accuracy may be needed. In the third structure, the accuracy of the approximate operating mode is improved by increasing the complexity of the approximate part whose internal structure is shown in Fig. 6(a). In this structure, the accuracy of output sum’ is increased. Similar to DQ4:2C1, the approximate part of this structure does not support output Cout. The error rate of this structure, however, is reduced to 50%.
4) Structure4(DQ4:2C4): In this structure, we improve the accuracy of the output carry’ compared with that of DQ4:2C3 at the cost of larger delay and power consumption where the error rate is reduced to 31.25%. The internal structure of the approximate part and the overall structure of DQ4:2C4 are shown in Fig. 7. The supplementary part is indicated by reddashed line rectangular while the gates of the approximate part, powered OFF during the exact operating mode, are indicated by the blue dotted line.
Advantages:

- Delay is less
- Power consumption is less

Software implementation:

- Modelsim
- Xilinx ISE