Low-Power Scan-Based Built-In Self-Test Based on Weighted Pseudorandom Test Pattern Generation and Reseeding

Abstract:

A new low-power (LP) scan-based built-in self-test (BIST) technique is proposed based on weighted pseudorandom test pattern generation and reseeding. A new LP scan architecture is proposed, which supports both pseudorandom testing and deterministic BIST. During the pseudorandom testing phase, an LP weighted random test pattern generation scheme is proposed by disabling a part of scan chains. During the deterministic BIST phase, the design-for-testability architecture is modified slightly while the linear-feedback shift register is kept short. In both the cases, only a small number of scan chains are activated in a single cycle. Sufficient experimental results are presented to demonstrate the performance of the proposed LP BIST approach. The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx 14.2.

Existing System:

Recent methods aim at reducing the switching activity during scan shift cycles, whose test generator allows automatic selection of their parameters for LP pseudorandom test generation. However, many of the previous LP BIST approaches cause fault coverage loss to some extent. Therefore, achieving high fault coverage in a LP BIST scheme is also very important. Weighted pseudorandom testing schemes and methods can effectively improve fault coverage. However, these approaches usually result in much more power consumption due to more frequent transitions at the scan flip flops in many cases. Therefore, we intend to propose an LP scan-based pseudorandom pattern generator (PRPG).

Scan flip flops, especially, the ones close to the scan-in pins, are not observable in most of shift cycles. Tsai et al. proposed a novel BIST scheme that inserts multiple capture cycles after scan shift cycles during a test cycle. Thus, the fault coverage of the scan-based BIST can be greatly improved. An improved method of the earlier work, presented, selects different numbers of capture cycles after the shift cycles. In this paper, a new LP scan-based BIST technique is
proposed based on weighted pseudorandom test pattern generation and reseeding. A new LP scan architecture is proposed, which supports both pseudorandom testing and deterministic BIST.

Weighted pseudorandom testing schemes can effectively improve fault coverage. A weighted test-enable signal-based pseudorandom test pattern generation scheme was proposed for scan-based BIST, according to which the number of shift cycles and the number of capture cycles in a single test cycle are not fixed. A reconfigurable scan architecture was used for the deterministic BIST scheme using the weighted test enable signal-based pseudorandom test generation scheme. Lai et al. proposed a new scan segmentation approach for more effective BIST. LP BIST approaches were proposed early, and Zorian proposed a distributed BIST control scheme in order to simplify the BIST execution of complex ICS. The average power was reduced and the temperature was reduced. The methods reduced switching activity during scan shifts by adding extra logic. A new random single-input change test generation scheme generates LP test patterns that provide a high level of defect coverage during LP BIST of digital circuits. An LP BIST scheme was proposed based on circuit partitioning.

New pseudorandom test generators were proposed to reduce power consumption during testing. A new encoding scheme is proposed, which can be used in conjunction with any LFSR-reseeding scheme to significantly reduce test power and even further reduce test data volume. Lai et al. [28] proposed a new LP PRPG for scan-based BIST using a restricted scan chain reordering method to recover the fault coverage loss.

A low-transition test pattern generator was proposed to reduce the average and peak power of a circuit during test by reducing the transitions among patterns. Transitions are reduced in two dimensions:

1) Between consecutive patterns

2) Between consecutive bits. Abu-Issa and Quigley proposed a PRPG to generate test vectors for test-per-scan BISTs in order to reduce the switching activity while shifting test vectors into the scan chain. Furthermore, a novel algorithm for scan-chain ordering has been presented.

**Disadvantages:**

- The data storage of chip is high
Proposed System:

New low-power weighted pseudorandom pattern test generator:

We propose a new LP scan-based BIST architecture, which supports LP pseudorandom testing, LP deterministic BIST and LP reseeding.

DFT Architecture:

As shown in Fig. 1, the scan-forest architecture is used for pseudorandom testing in the first phase. Each stage of the phase shifter (PS) drives multiple scan chains, where all scan chains in the same scan tree are driven by the same stage of the PS. Unlike the multiple scan-chain architecture used in the previous methods, the scan-forest architecture is adopted to compress test data and reduce the deterministic test data volume. Separate weighted signals $s_0, e_1, ..., e_n$ are assigned to all scan chains in the weighted pseudorandom testing phase (phase=0), as shown in Fig. 1, which is replaced by the regular test in the deterministic BIST phase (phase=1). Each scan-in signal drives multiple scan chains, as shown in Fig. 1, where different scan chains are assigned different weights. This technique can also significantly reduce the size of the PS compared with the multiple scan-chain architecture where each stage of the PS drives one scan chain. The compactor connected to the combinational part of the circuit is to reduce the size of the MISR. The shadow register is used for LP deterministic and reseeding.
The size of the LFSR needed for deterministic BIST depends on the maximum number of care bits of all deterministic test vectors for most of the previous deterministic BIST methods. In some cases, the size of the LFSR can be very large because of a few vectors with a large number of care bits even when a well-designed PS is adopted. This may significantly increase the test data volume in order to keep these seeds. This problem can be solved by adding a small number of extra variables to the LFSR or ring generator without keeping a big seed for each vector.

Weighted Pseudorandom Test Pattern Generation:

Our method generates the degraded sub circuits for all subsets of scan chains in the following way. All PPIs related to the disabled scan chains are randomly assigned specified values (1 and 0). Note that all scan flip flops at the same level of the same scan tree share the same PPI. For any gate, the gate is removed if its output is specified; the input can be removed from a NAND, NOR, AND, and OR gates if the input is assigned a non-controlling value and it has at least three inputs. For a two-input AND or OR gate, the gate is removed if one of its inputs is assigned a non-
controlling value. For a NOR or NAND gate, the gate degrades to an inverter if one of its inputs is assigned a non-controlling value.

For an XOR or NXOR gate with more than three inputs, the input is simply removed from the circuit if one of its inputs is assigned value 0; the input is removed if it is assigned value 1, an XOR gate changes to an NXOR gate, and an NXOR gate changes to an XOR gate. For an XOR gate with two inputs, and one of its inputs is assigned value 0, the gate is deleted from the circuit. For a two-input NXOR gate, the gate degrades to an inverter. If one of its inputs is assigned value 1, a two-input XOR gate degrades to an inverter. If one of its inputs is assigned value 1, a two-input NXOR gate can be removed from the circuit.

In the scan-based BIST architecture, as shown in Fig. 2, different weights, e0, e1,..., and ek are assigned to the testenable signals of the scan chains SC0, SC1,..., and SCk, respectively, where e0,
Scan flip flops in all disabled scan chains are set to constant values. Our method randomly assigns constant values to all scan flip flops in the disabled scan chains. The circuit is degraded into a smaller sub-circuit. All weights on the testenable signals are selected in the degraded sub-circuit.

The gating logic is presented in Fig. 1. We do not assign weights less than 0.5 to the test-enable signals, because we do not want to insert more capture cycles than scan shift cycles. We have developed an efficient method to select weights for the test-enable signals of the scan chains.

**Advantages:**

- Reduce the data storage on chip

**Software implementation:**

- Modelsim
- Xilinx ISE